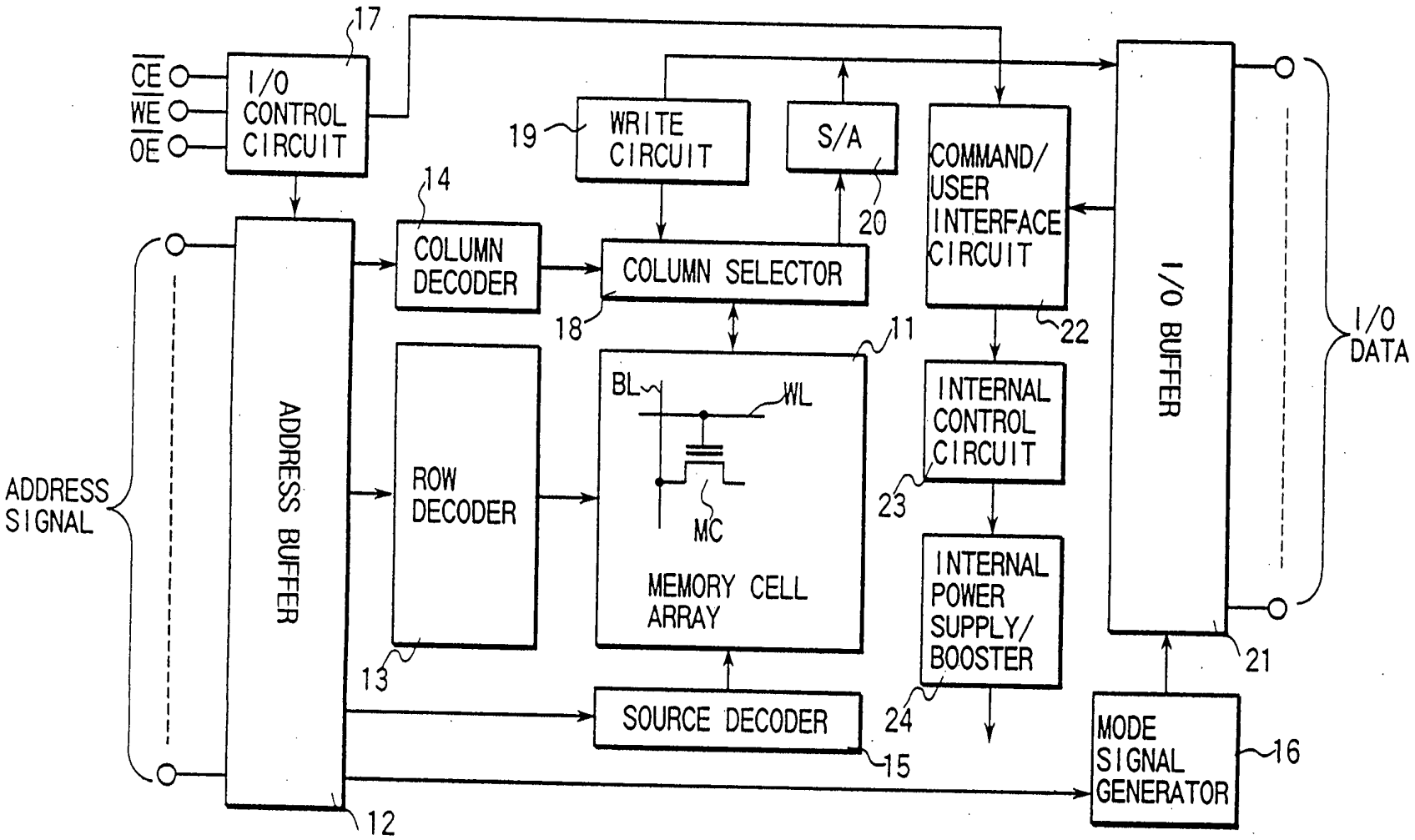

CE
WE
OE
I/O CONTROL CIRCUIT
17
19
WRITE CIRCUIT
S/A
20
COMMAND/ USER INTERFACE CIRCUIT
I/O BUFFER
I/O DATA
14
COLUMN DECODER
COLUMN SELECTOR
18
22
11
ADDRESS SIGNAL
ADDRESS BUFFER
ROW DECODER
BL
WL
MC
MEMORY CELL ARRAY
INTERNAL CONTROL CIRCUIT
23
INTERNAL POWER SUPPLY/ BOOSTER
24
13
SOURCE DECODER
15
MODE SIGNAL GENERATOR
16
21
12

FIG. 1

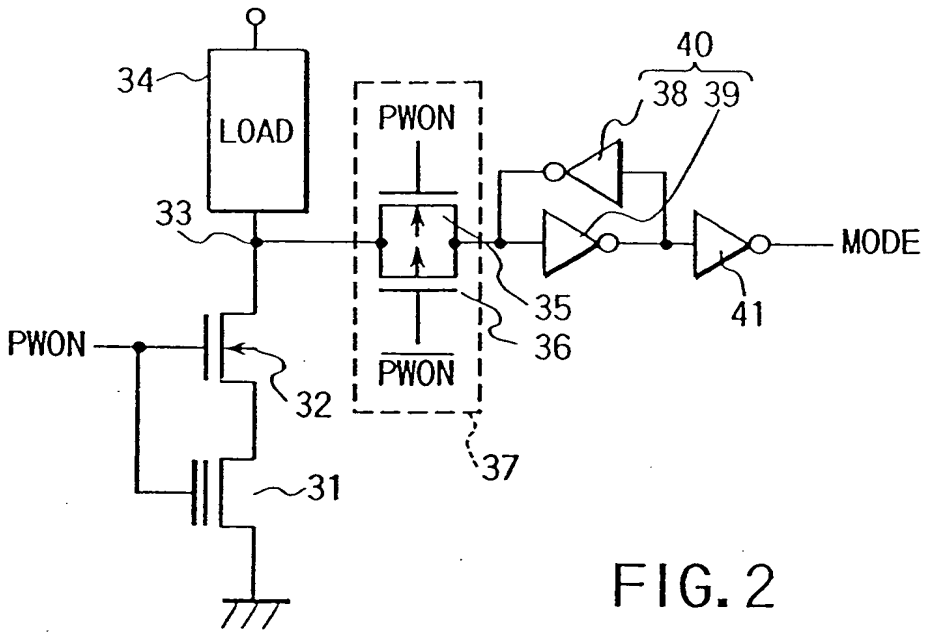

34
LOAD
33
PWON
32
31
PWON
PWON
35
36
37
40
38
39
41
MODE

FIG. 2

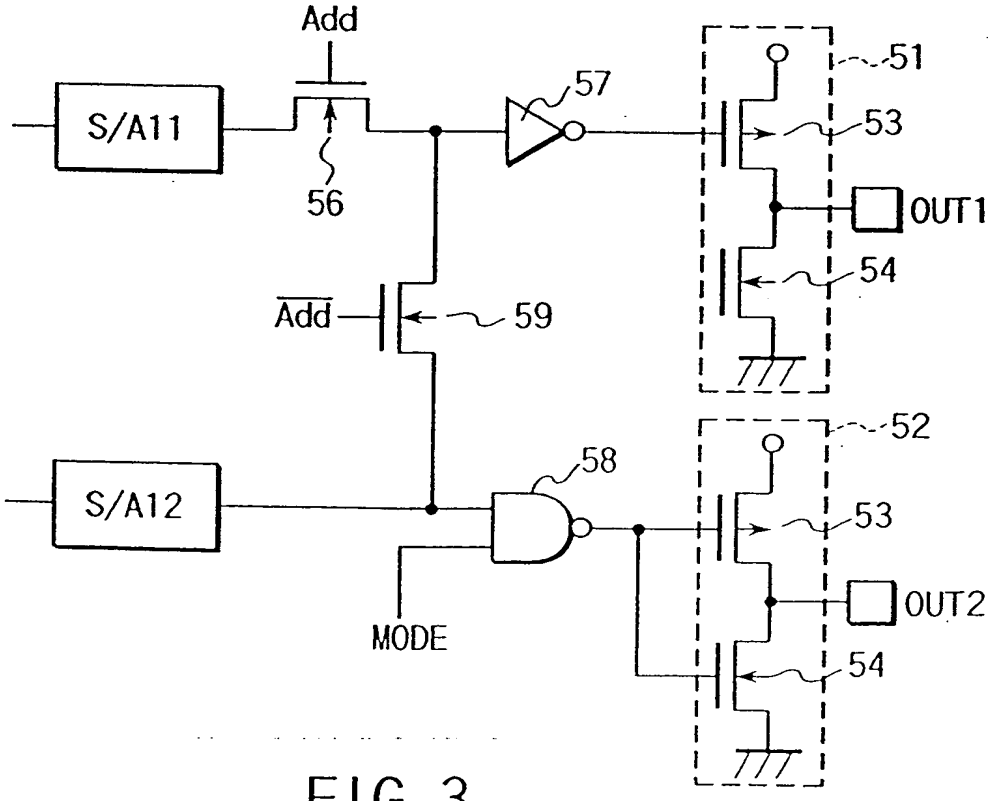

Add
S/A11
56
57
51
53
OUT1
54
Add
59
S/A12
58
52
53
OUT2
54
MODE

FIG. 3

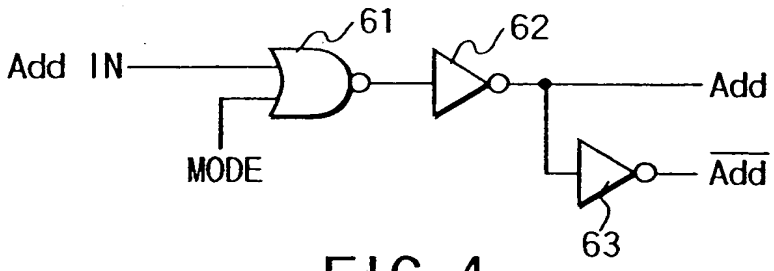



FIG. 4

| | Vg | Vd | Vs |
|---|---|---|---|
| WRITE | 10V | 6V | 0V |
| ERASE | -7V | OPEN | 6V |
| READ | 5V | 1V | 0V |

FIG. 5

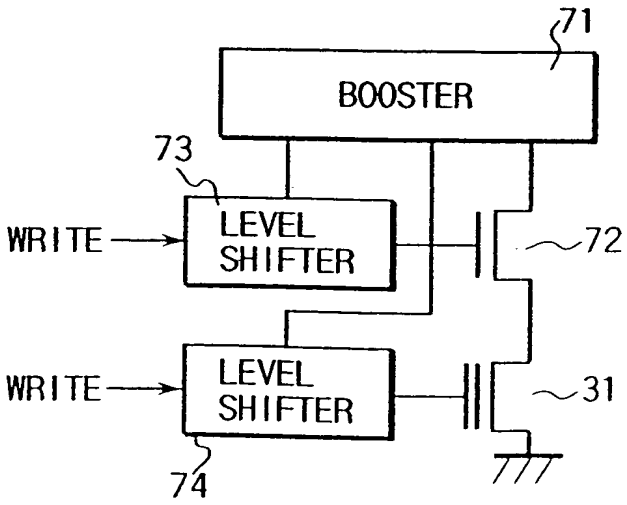



FIG. 6A

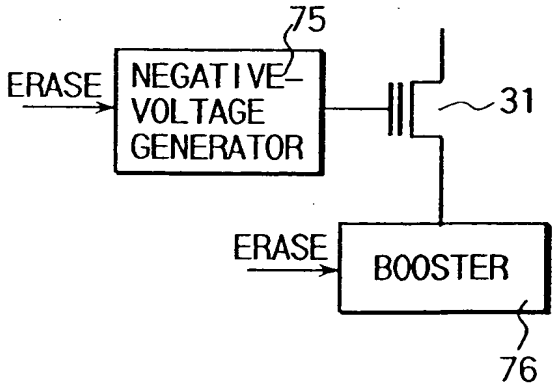



FIG. 6B

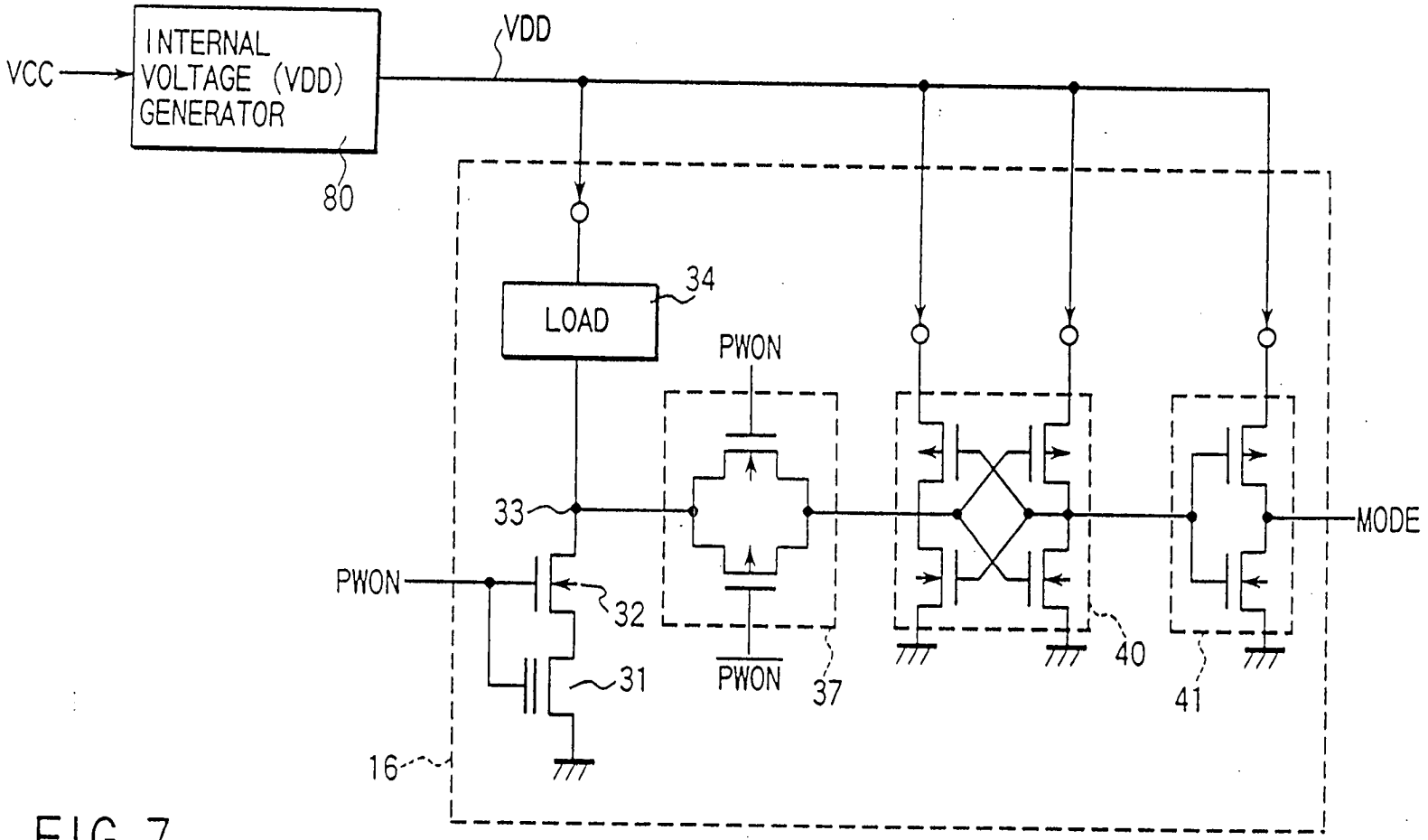

VCC
INTERNAL VOLTAGE (VDD) GENERATOR
80
VDD
LOAD
34
PWON
33
PWON
32
31
16
PWON
37
40
41
MODE

FIG. 7

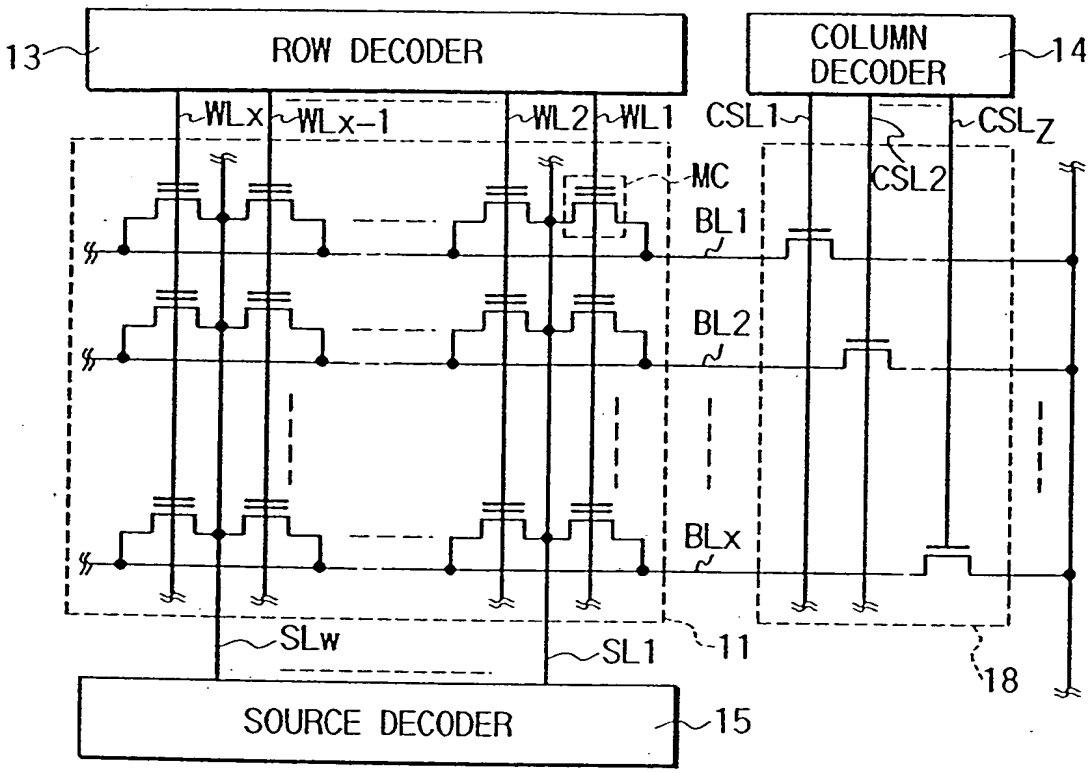



FIG. 8A

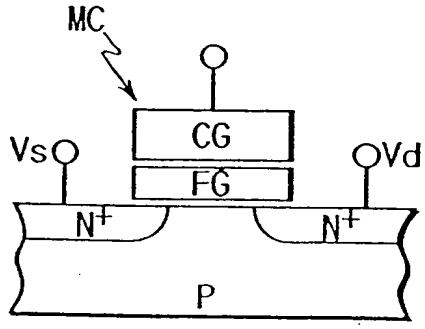



FIG. 8B

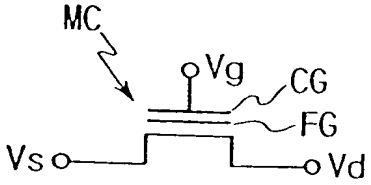



FIG. 8C

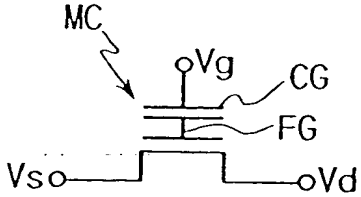



FIG. 8D

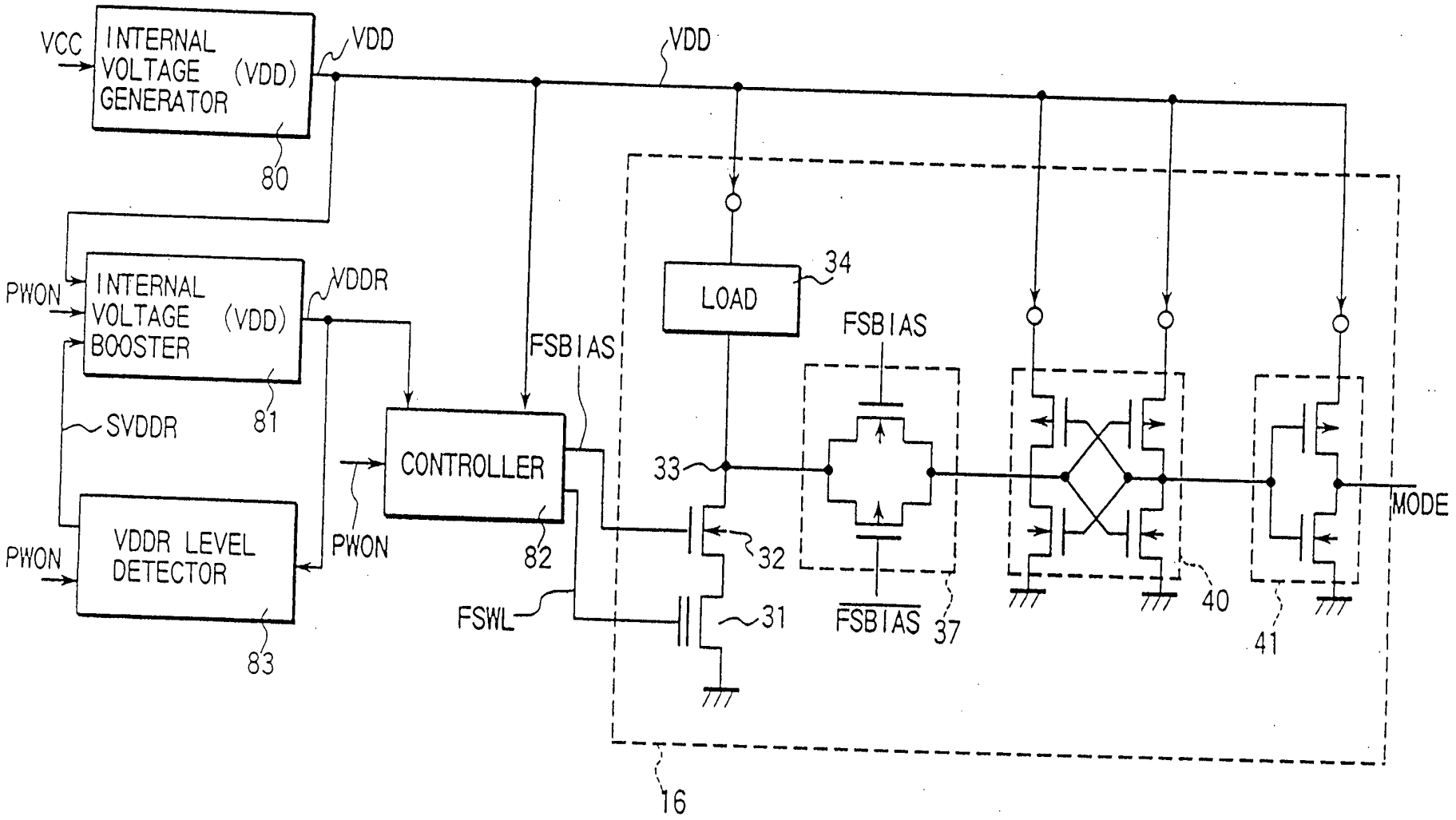

VCC
INTERNAL VOLTAGE GENERATOR (VDD)
80
VDD
VDD
PWON
INTERNAL VOLTAGE BOOSTER (VDD)
81
VDDR
SVDDR
CONTROLLER
82
FSBIAS
PWON
PWON
VDDR LEVEL DETECTOR
83
LOAD
34
FSBIAS
33
32
FSWL
31
FSBIAS
37
40
41
MODE
16

FIG. 9

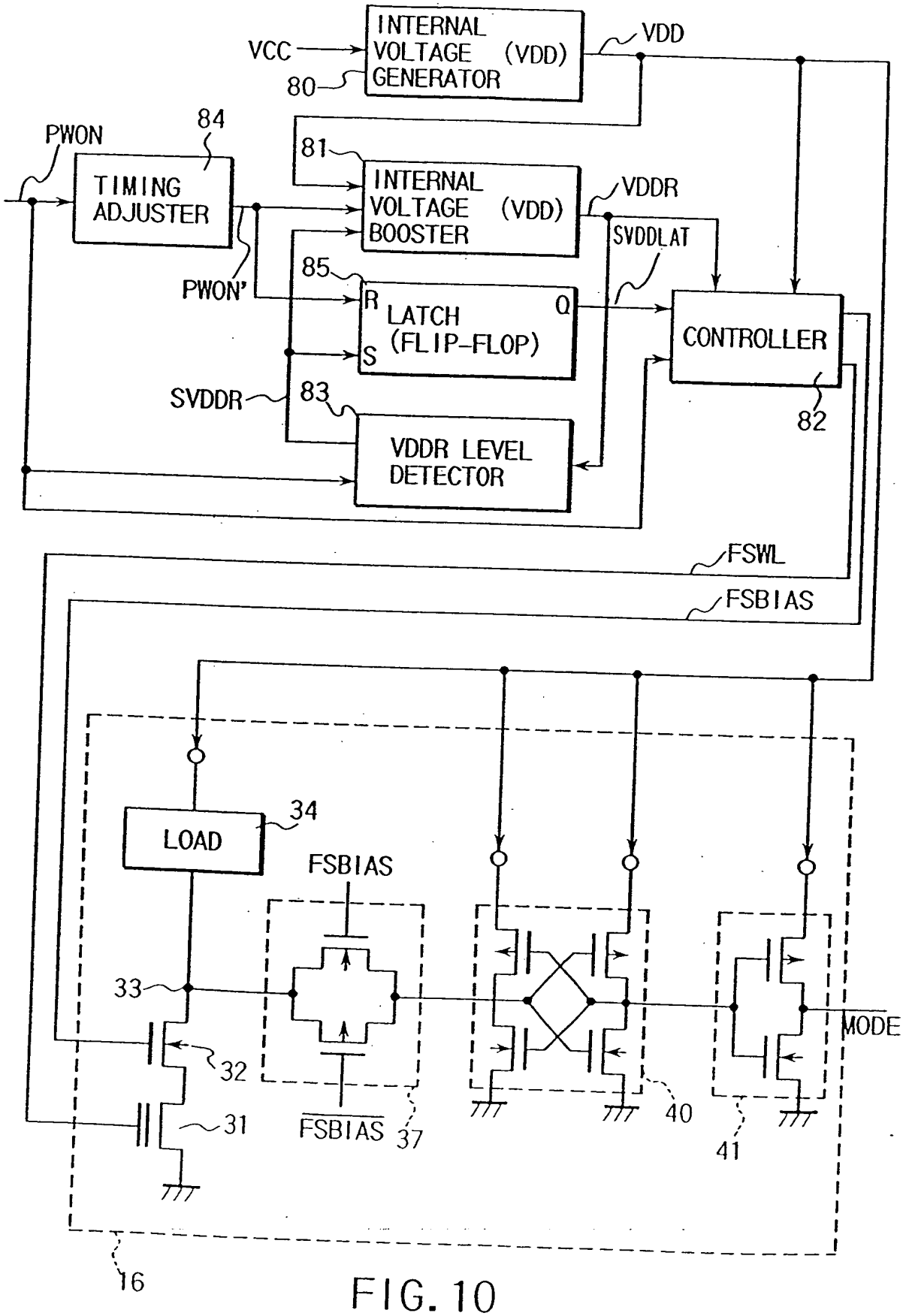

INTERNAL VOLTAGE (VDD) GENERATOR
VCC
80
VDD
PWON
84
TIMING ADJUSTER
81
INTERNAL VOLTAGE (VDD) BOOSTER
VDDR
SVDDLAT
PWON'
85
R
LATCH (FLIP-FLOP)
Q
S
CONTROLLER
82
SVDDR
83
VDDR LEVEL DETECTOR
FSWL
FSBIAS
LOAD
34
FSBIAS
33
32
31
FSBIAS
37
40
41
MODE
16

FIG. 10

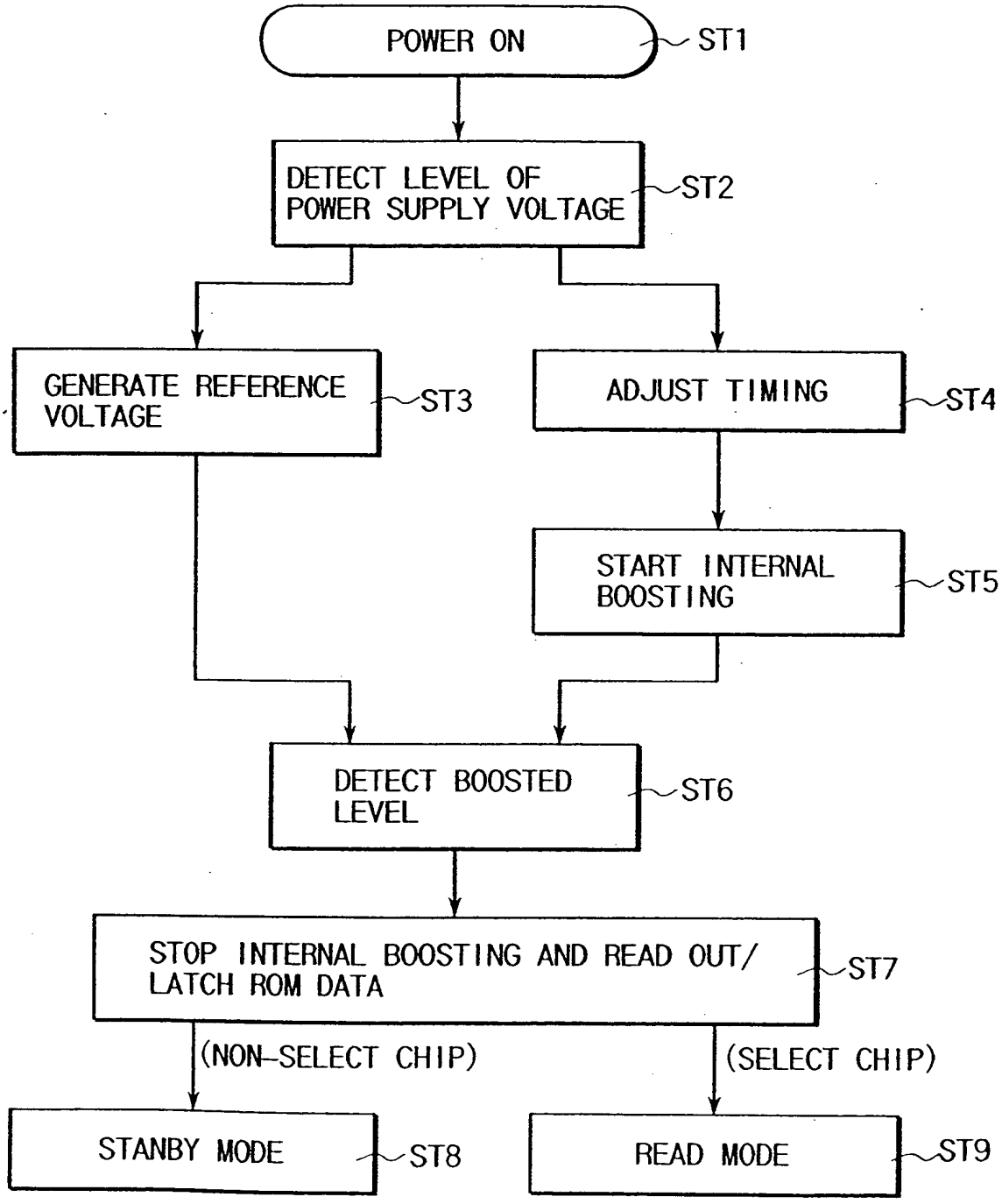

POWER ON
ST1
DETECT LEVEL OF POWER SUPPLY VOLTAGE
ST2
GENERATE REFERENCE VOLTAGE
ST3
ADJUST TIMING
ST4
START INTERNAL BOOSTING
ST5
DETECT BOOSTED LEVEL
ST6
STOP INTERNAL BOOSTING AND READ OUT/ LATCH ROM DATA
ST7
(NON-SELECT CHIP)
(SELECT CHIP)
STANBY MODE
ST8
READ MODE
ST9

FIG. 11

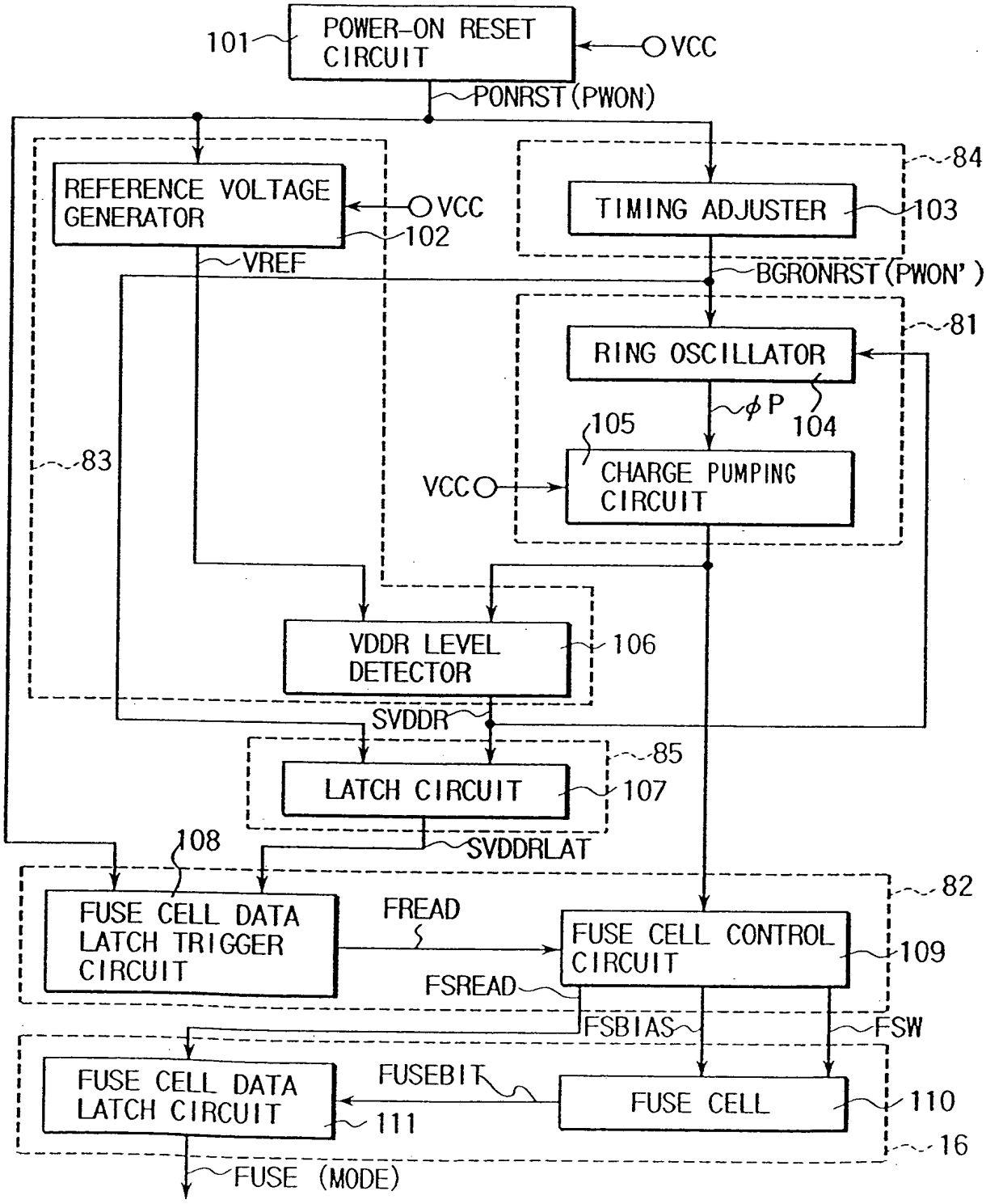

101
POWER-ON RESET CIRCUIT
VCC
PONRST(PWON)
84
REFERENCE VOLTAGE GENERATOR
VCC
102
TIMING ADJUSTER
103
VREF
BGRONRST(PWON')
81
RING OSCILLATOR
φP
104
105
83
VCC
CHARGE PUMPING CIRCUIT
VDDR LEVEL DETECTOR
106
SVDDR
85
LATCH CIRCUIT
107
SVDDRLAT
108
82
FUSE CELL DATA LATCH TRIGGER CIRCUIT
FREAD
FUSE CELL CONTROL CIRCUIT
109
FSREAD
FSBIAS
FSW
FUSE CELL DATA LATCH CIRCUIT
FUSEBIT
FUSE CELL
110
111
16
FUSE (MODE)

FIG. 12

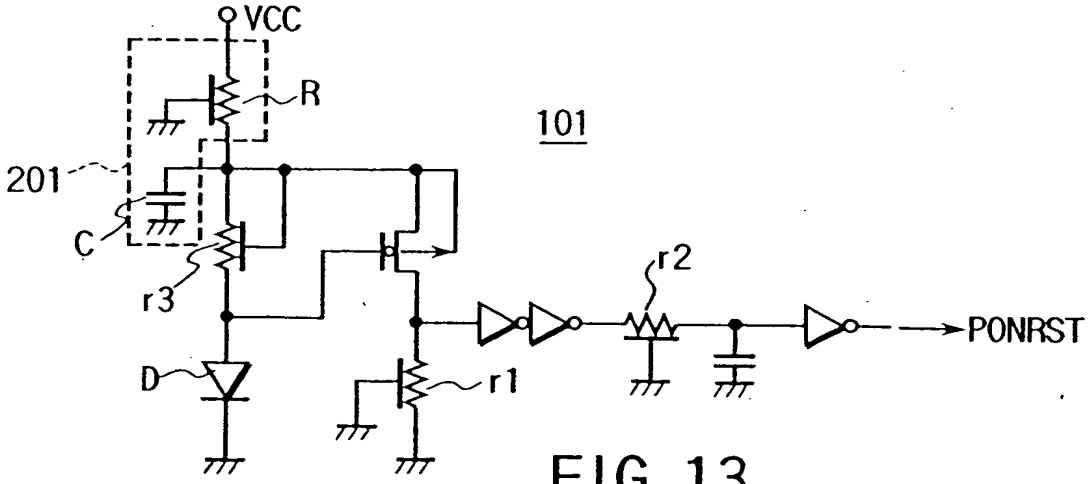



FIG. 13

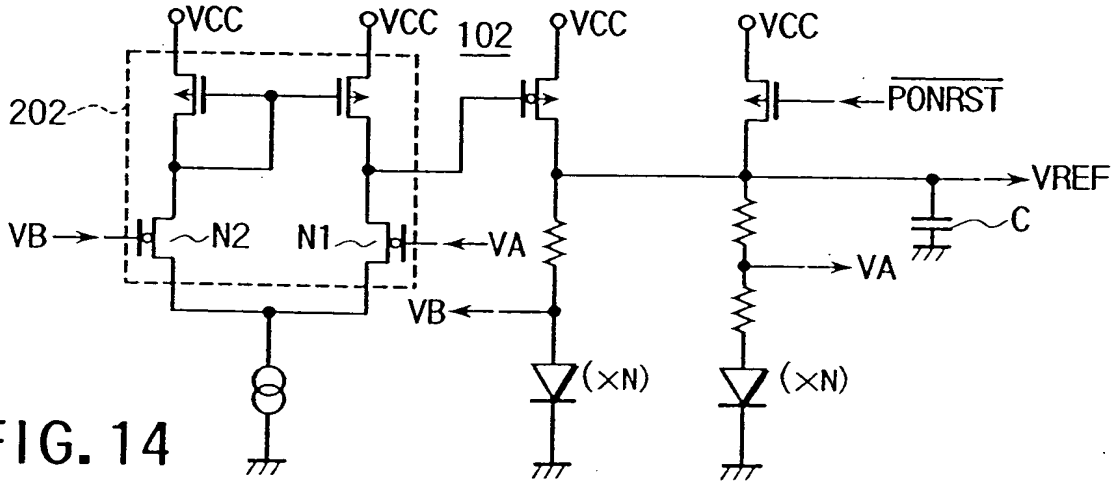



FIG. 14

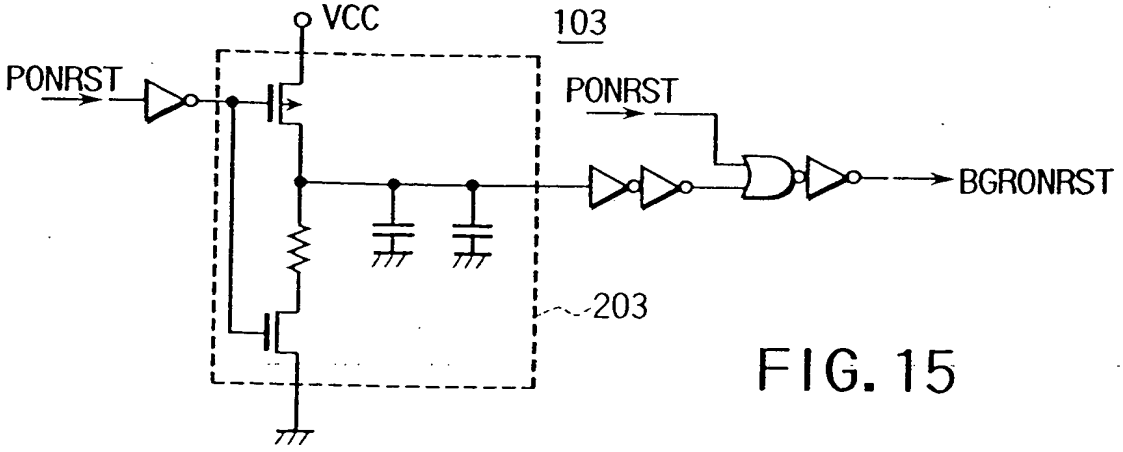



FIG. 15

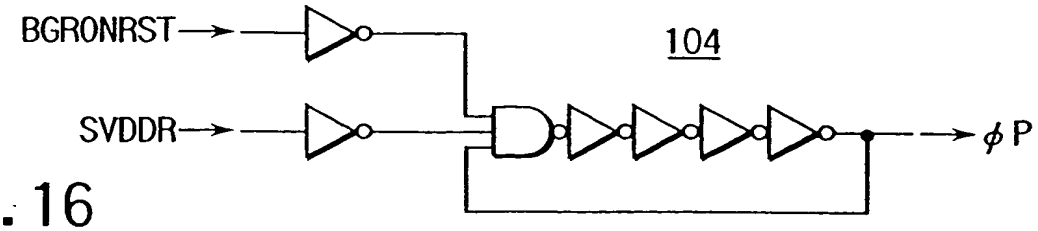



FIG. 16

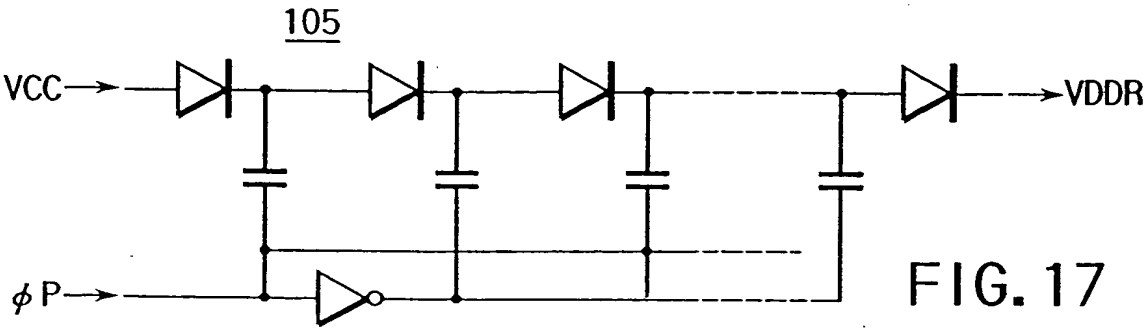



FIG. 17

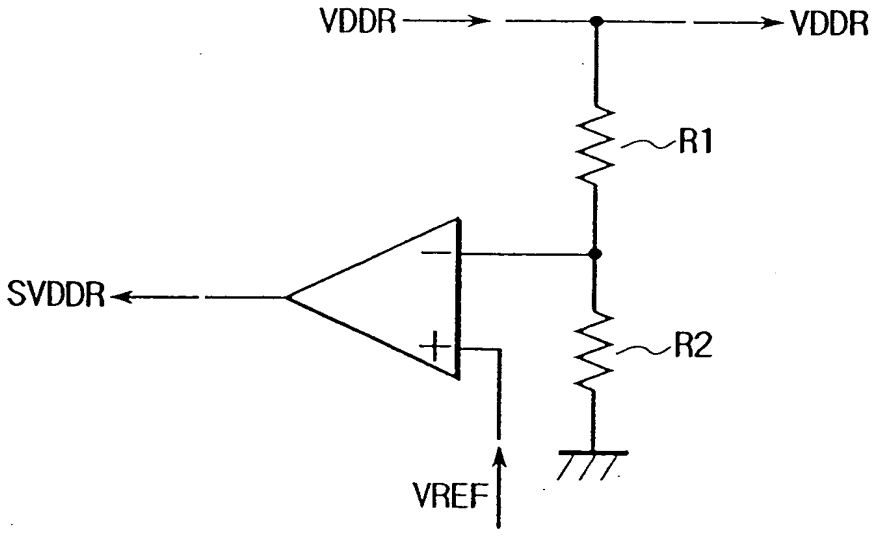



FIG. 18

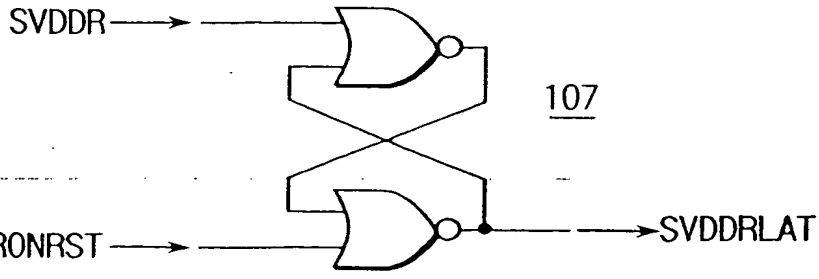



FIG. 19

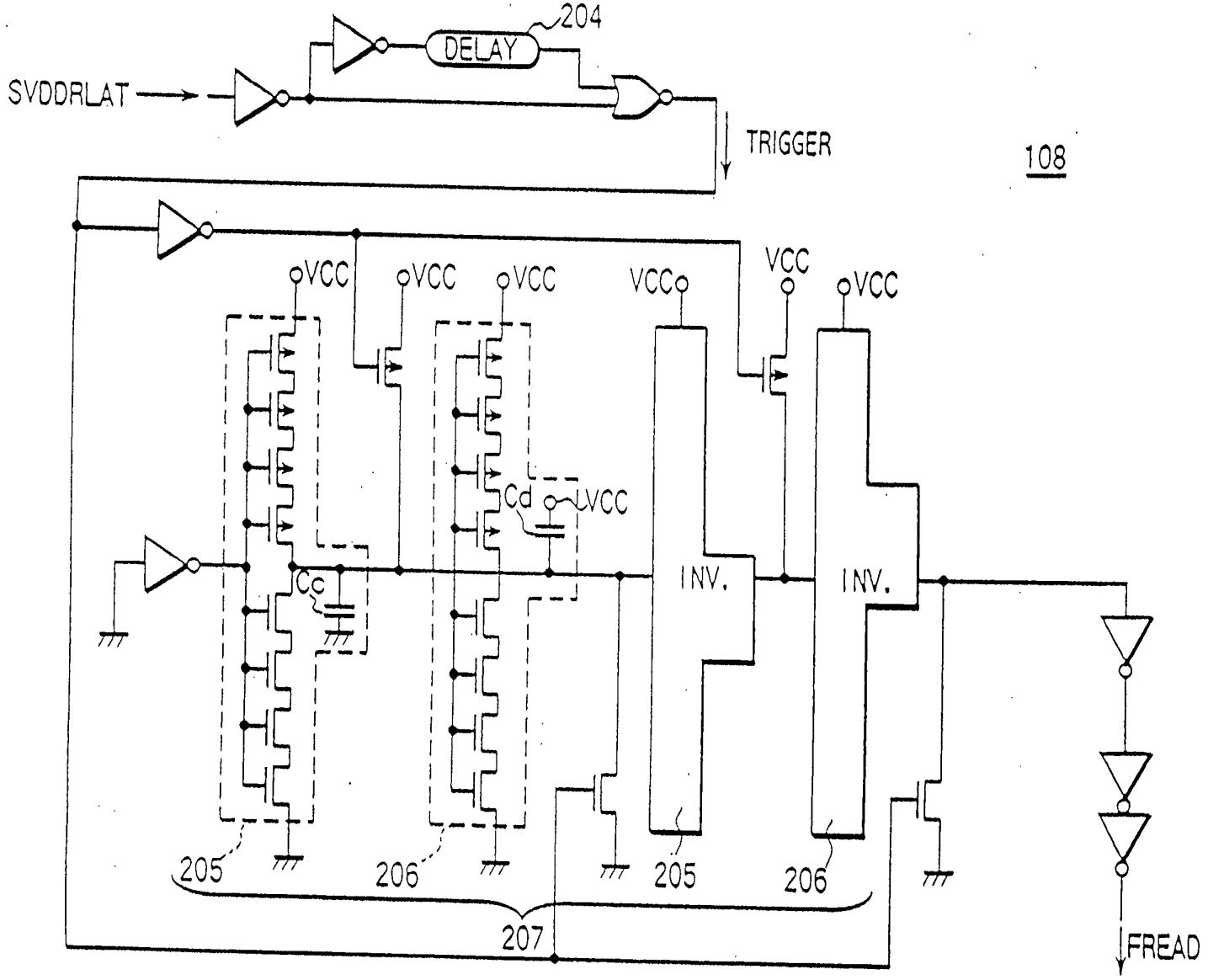

204
DELAY
SVDDRLAT
TRIGGER
108
VCC
VCC
VCC
VCC
VCC
VCC
Cd
VCC
Cc
INV.
INV.
205
206
205
206
207
FREAD

FIG. 20

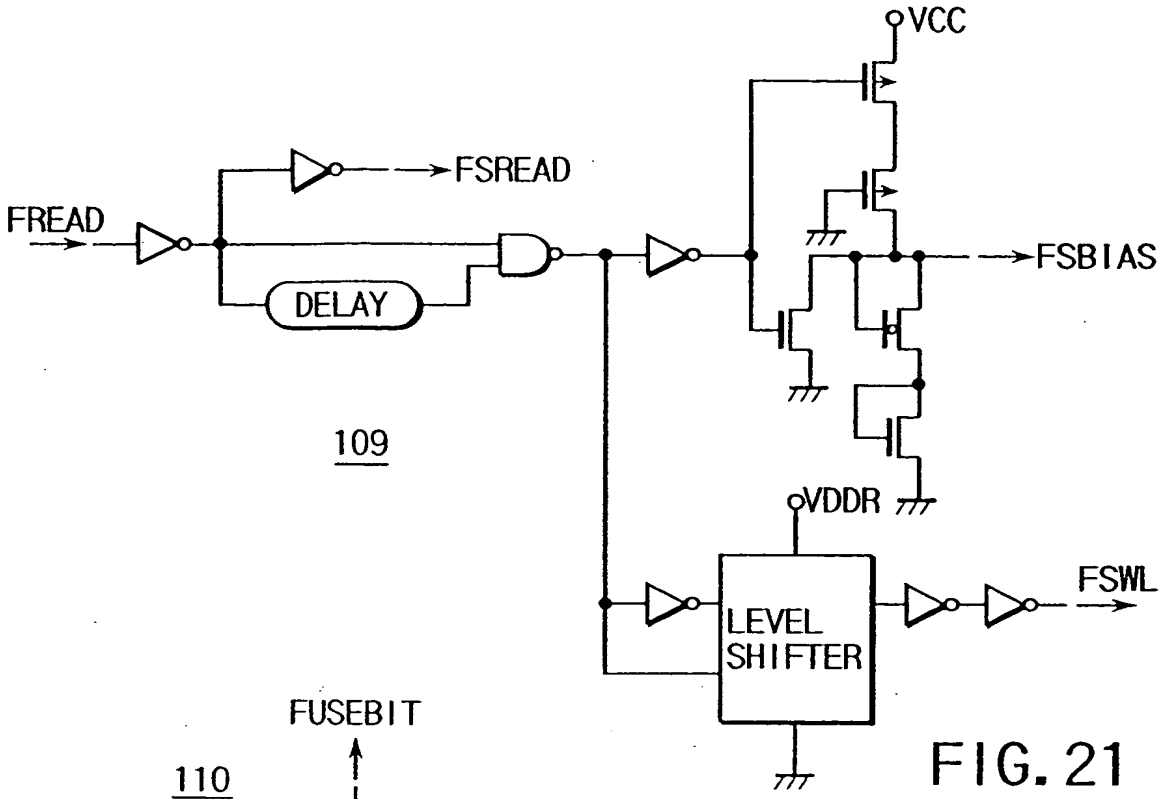



FIG. 21

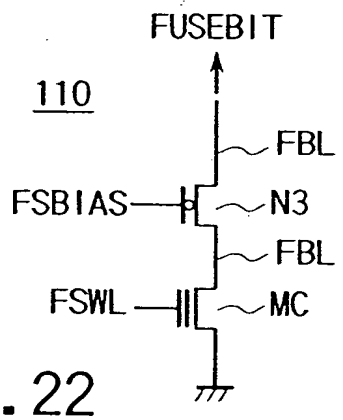



FIG. 22

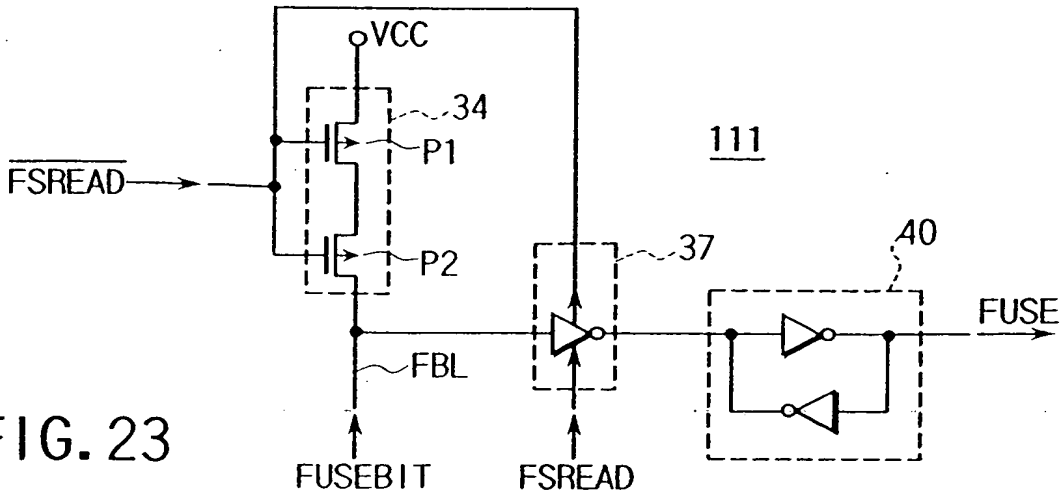



FIG. 23

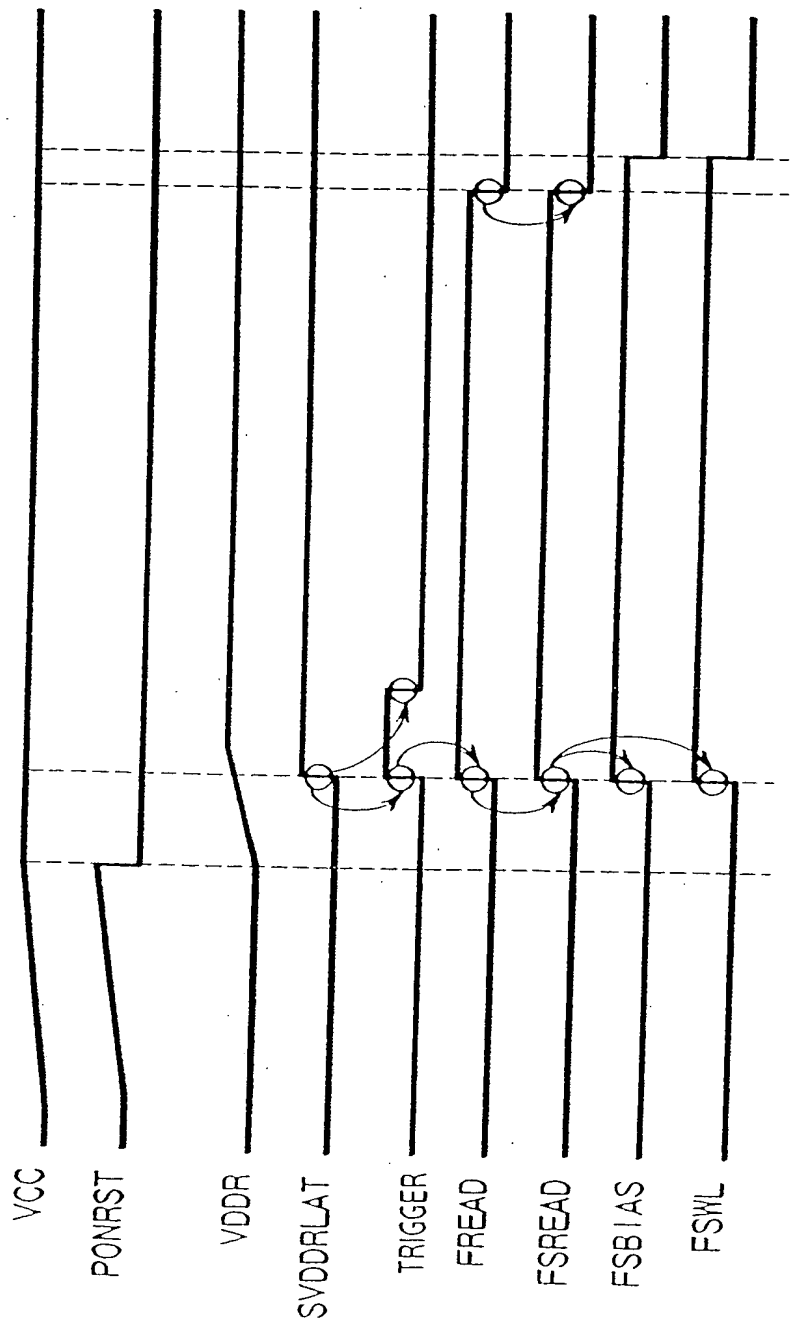



FIG. 24

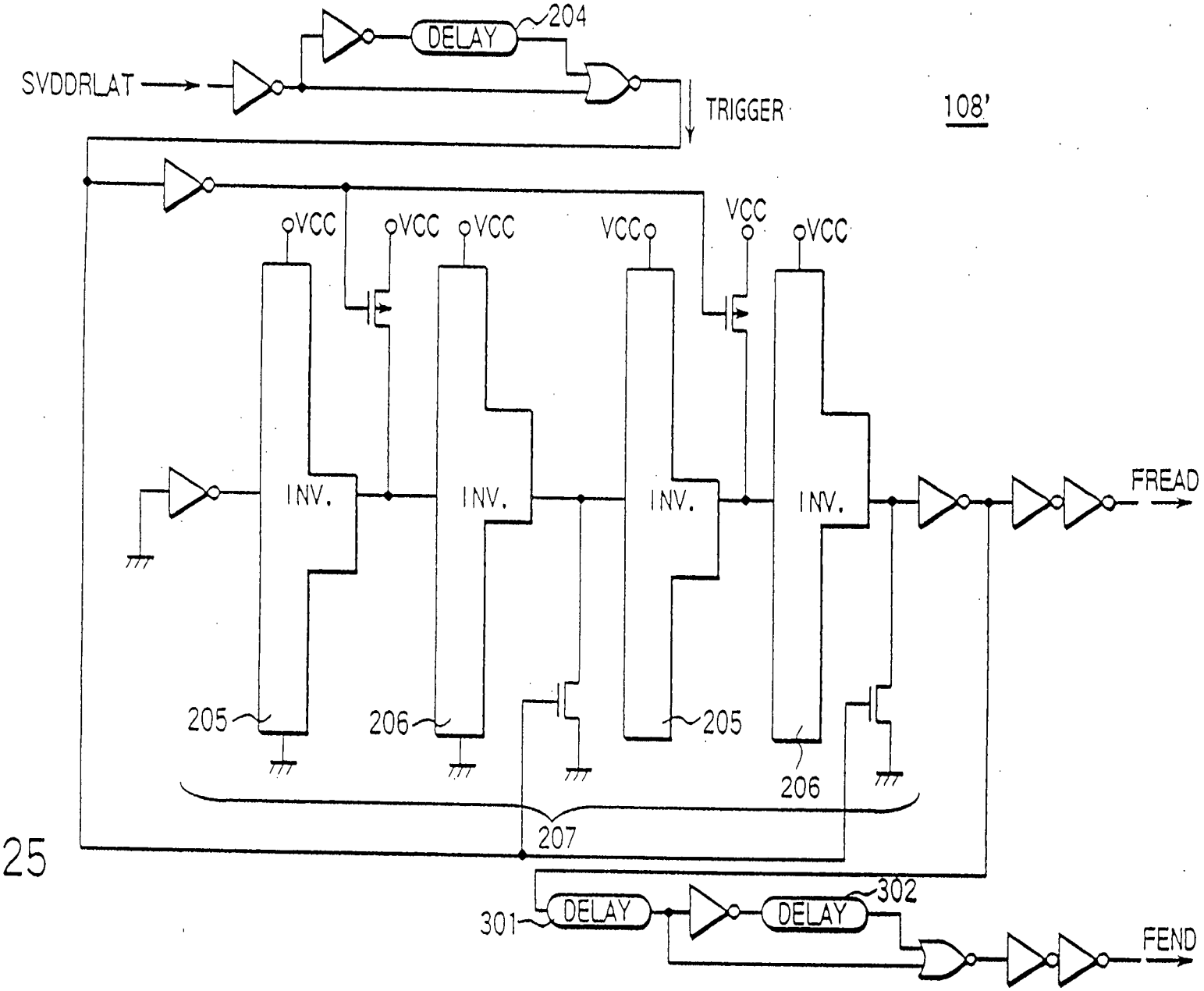

SVDDRLAT
DELAY
204
TRIGGER
108'
VCC
VCC
VCC
VCC
VCC
VCC
INV.
INV.
INV.
INV.
FREAD
205
206
205
206
207
301
DELAY
DELAY
302
FEND

FIG. 25

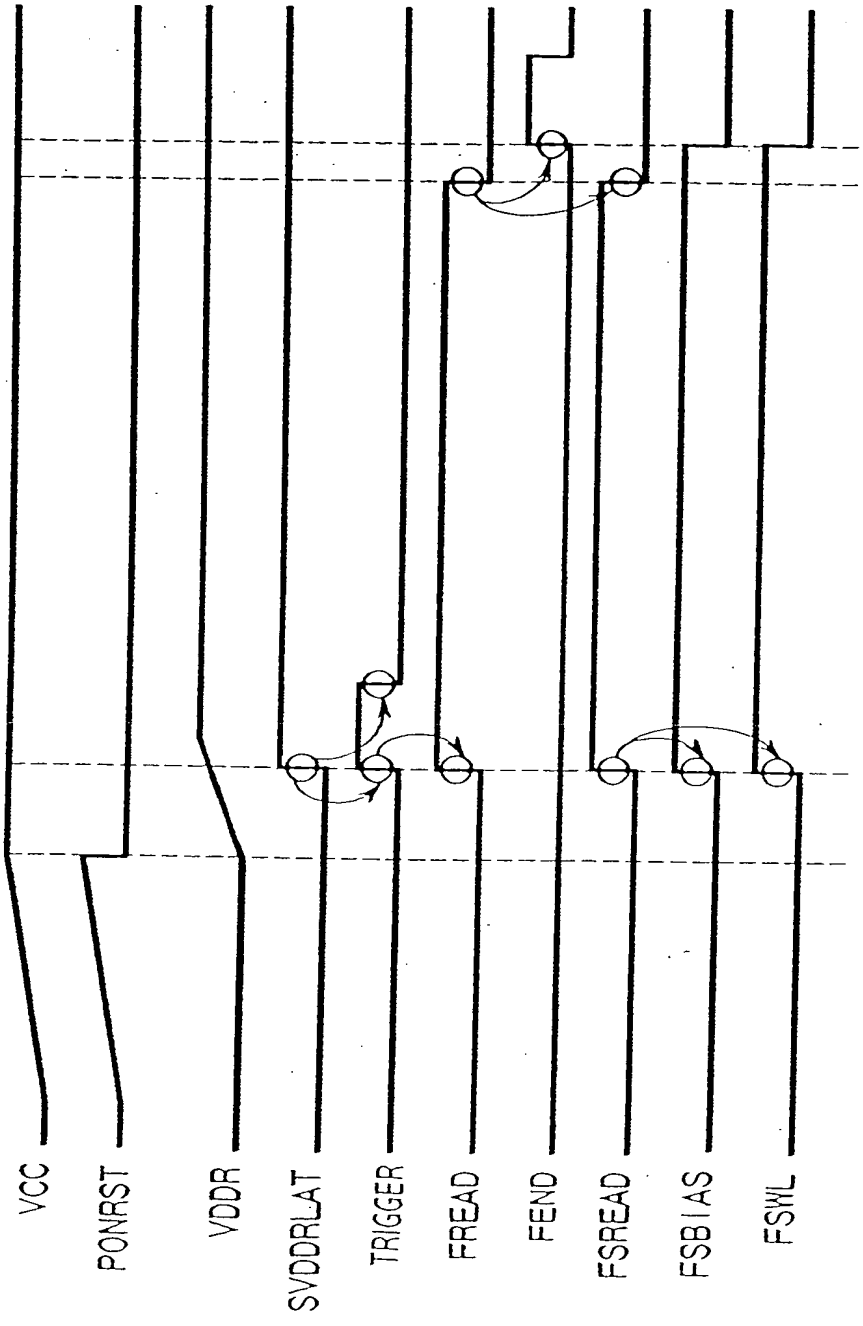

VCC
PONRST
VDDR
SVDDRLAT
TRIGGER
FREAD
FEND
FSREAD
FSBIAS
FSWL

FIG. 26

FIG. 27A

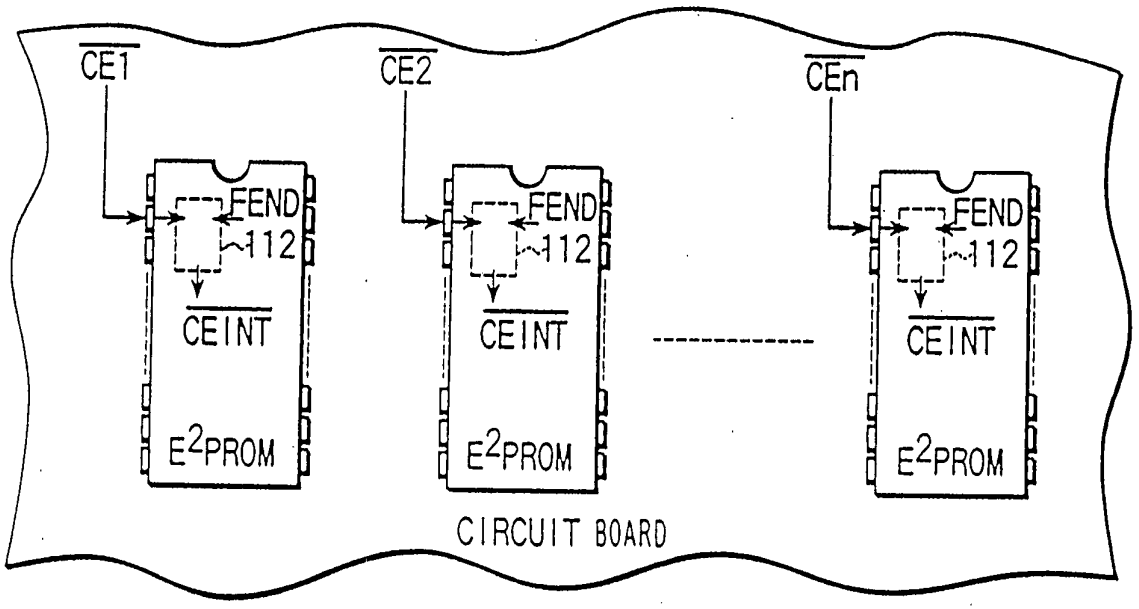
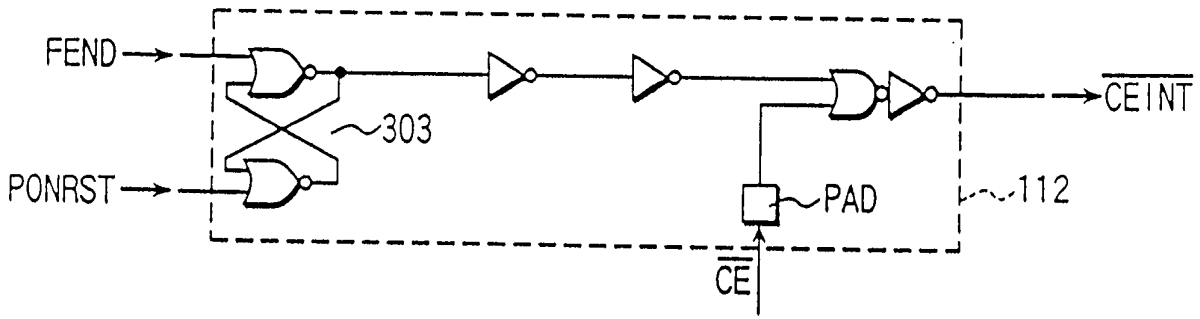



FIG. 27B



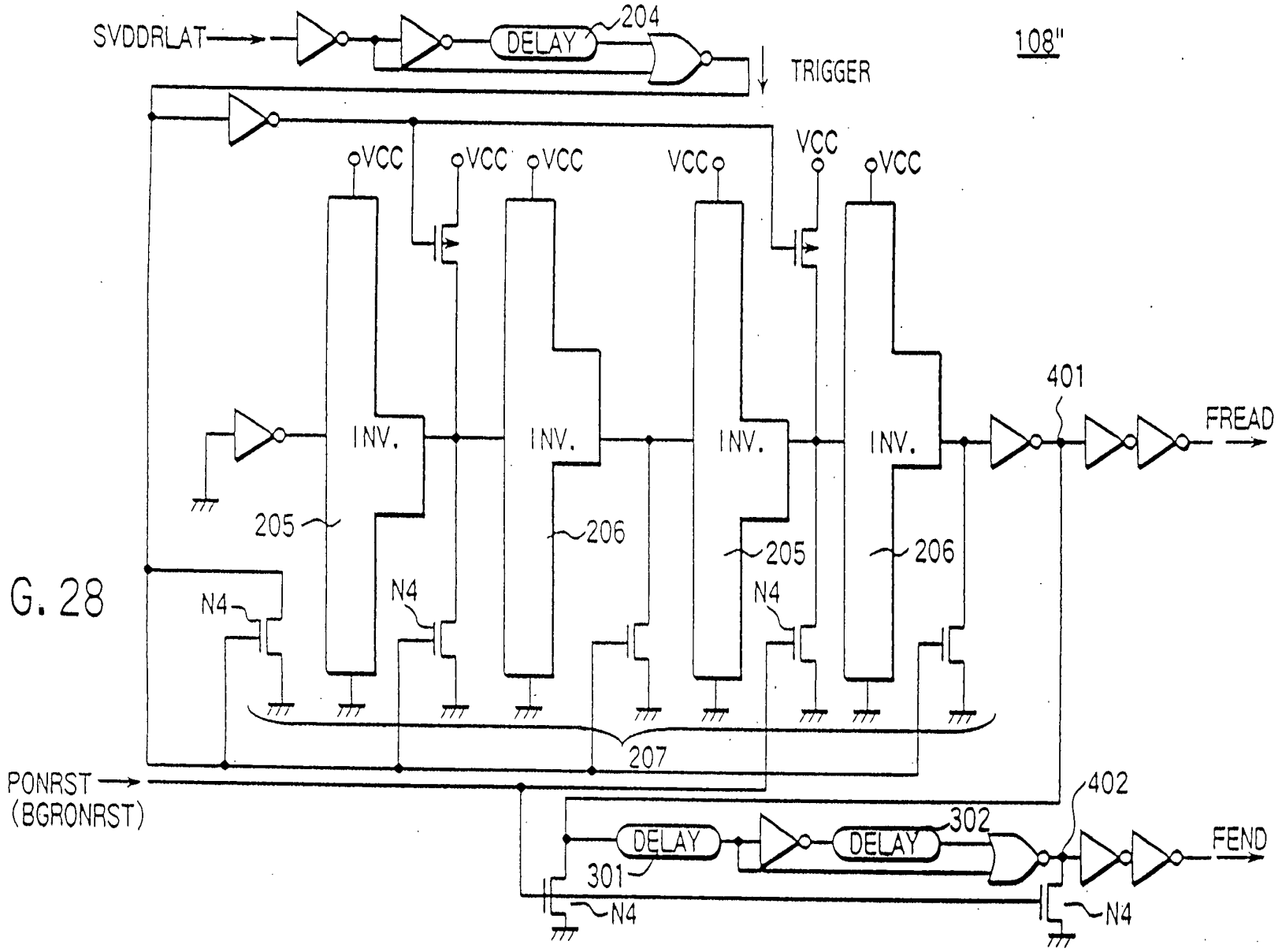

SVDDRLAT
DELAY
204
TRIGGER
108"
VCC
VCC
VCC
VCC
VCC
VCC
INV.
INV.
INV.
INV.
401
FREAD
205
206
205
206
N4
N4
N4
207
PONRST
(BGRONRST)
402
DELAY
DELAY
302
FEND
301
N4
N4

FIG. 28

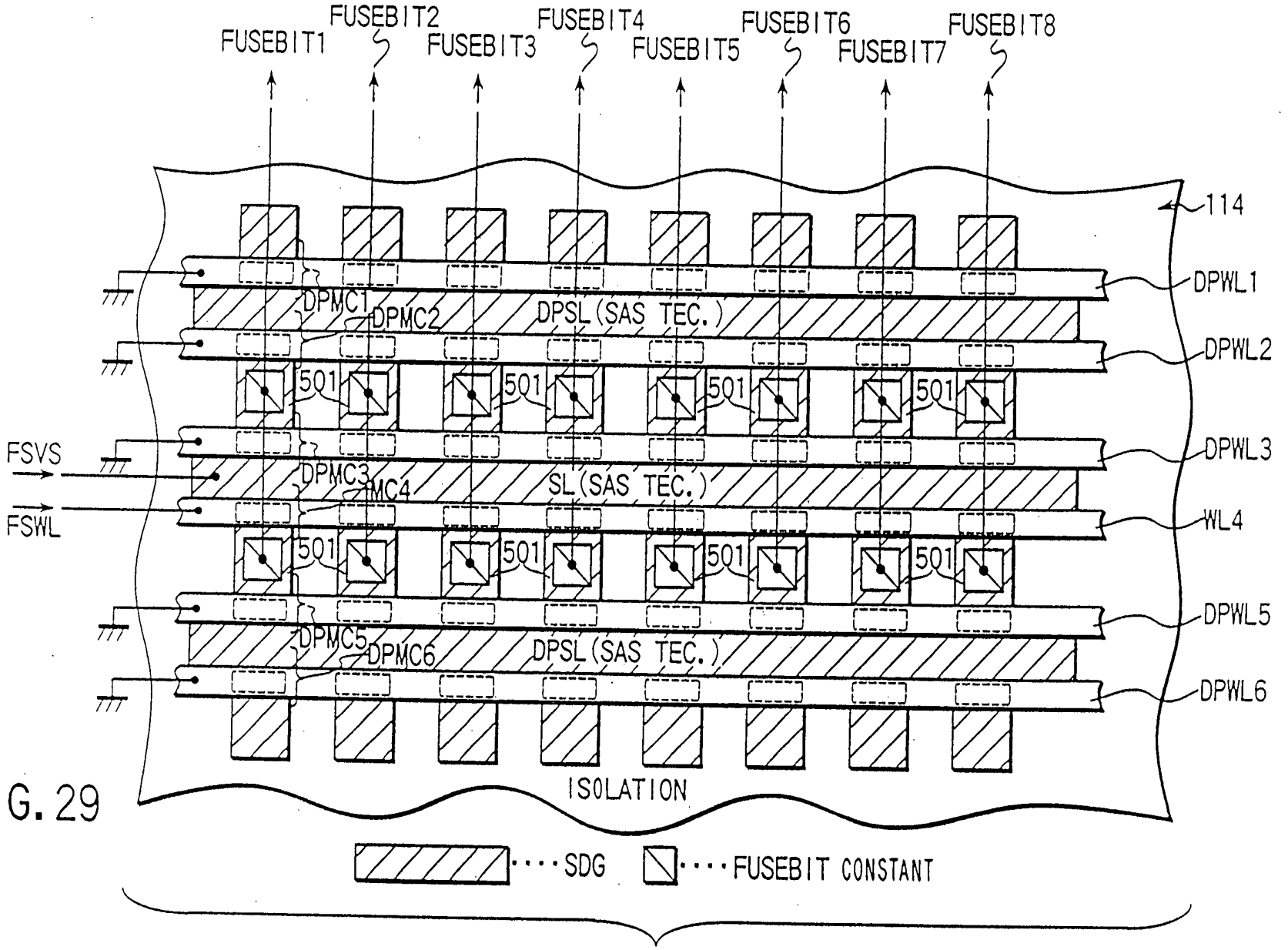

FUSEBIT1
FUSEBIT2
FUSEBIT3
FUSEBIT4
FUSEBIT5
FUSEBIT6
FUSEBIT7
FUSEBIT8
114
DPWL1
DPWL2
DPWL3
WL4
DPWL5
DPWL6
DPMC1
DPMC2
DPSL (SAS TEC.)
501
FSVS
FSWL
DPMC3
MC4
SL (SAS TEC.)
DPMC5
DPMC6
DPSL (SAS TEC.)
ISOLATION
SDG
FUSEBIT CONSTANT

FIG. 29

FIG. 30

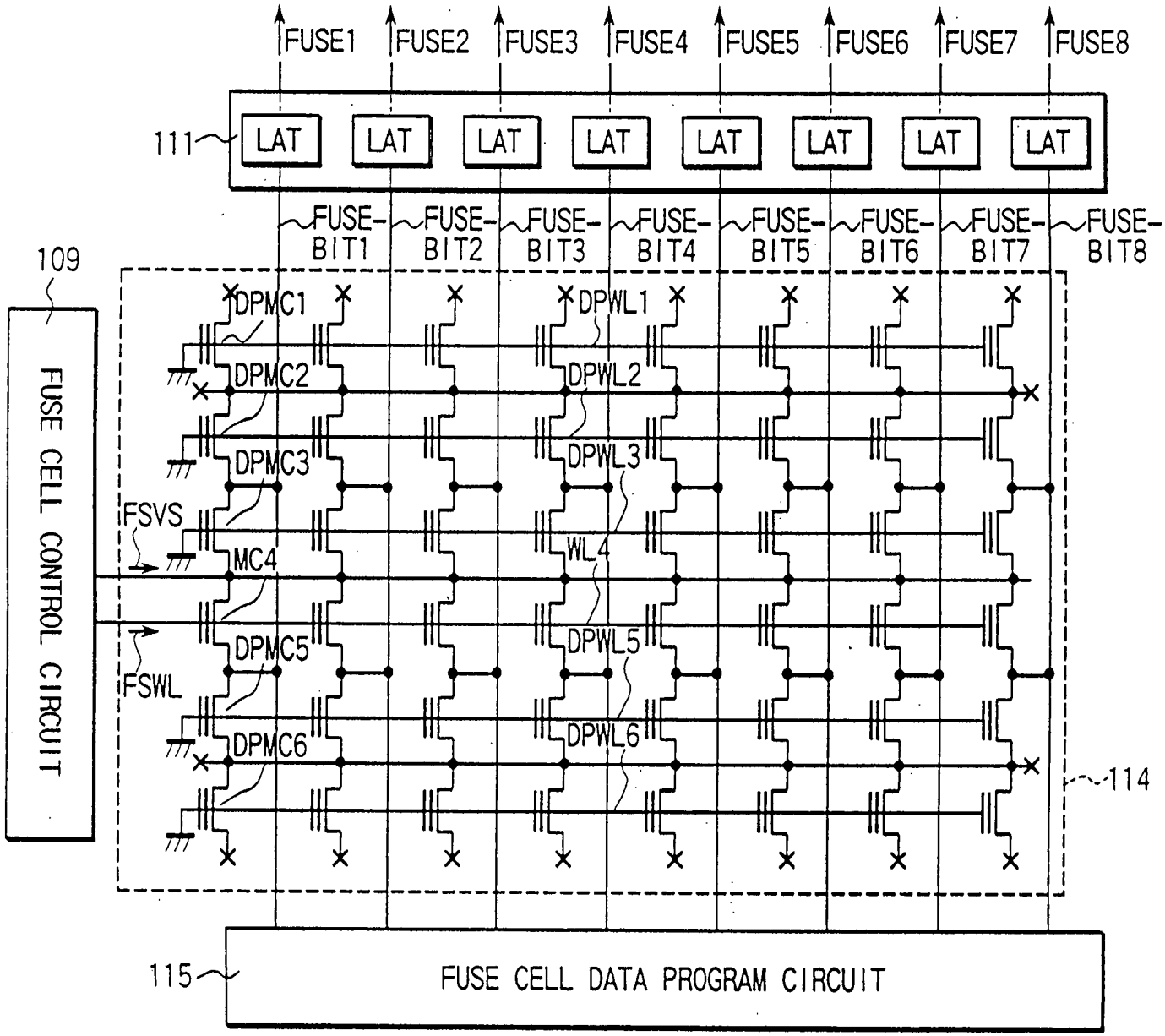
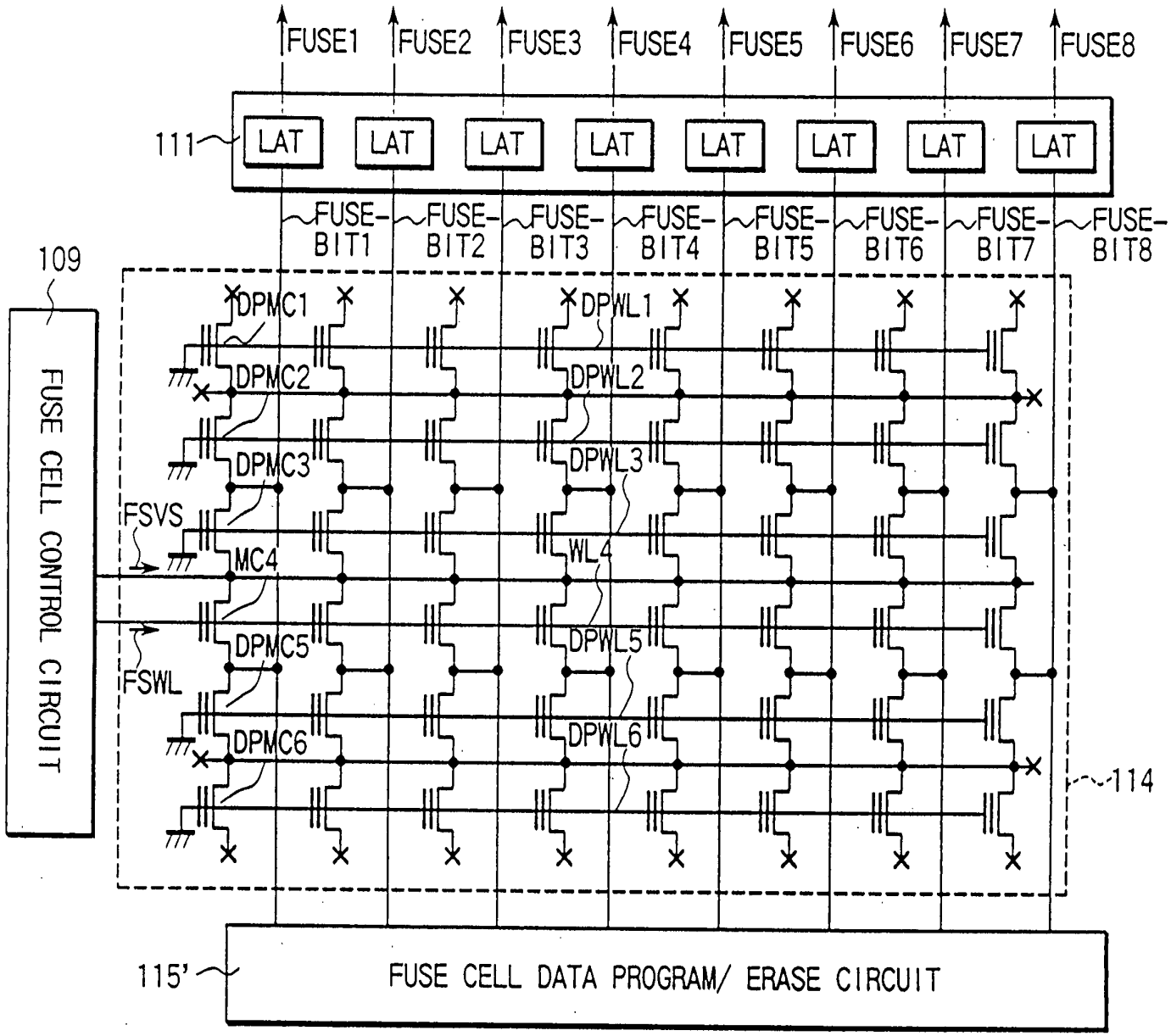

FUSE1
FUSE2
FUSE3
FUSE4
FUSE5
FUSE6
FUSE7
FUSE8
111
LAT
FUSE-BIT1
FUSE-BIT2
FUSE-BIT3
FUSE-BIT4
FUSE-BIT5
FUSE-BIT6
FUSE-BIT7
FUSE-BIT8
109
FUSE CELL CONTROL CIRCUIT
DPMC1
DPMC2
DPMC3
FSVS
MC4
FSWL
DPMC5
DPMC6
DPWL1
DPWL2
DPWL3
WL4
DPWL5
DPWL6
114
115
FUSE CELL DATA PROGRAM CIRCUIT

FIG. 31


FUSE1
FUSE2
FUSE3
FUSE4
FUSE5
FUSE6
FUSE7
FUSE8
111
LAT
LAT
LAT
LAT
LAT
LAT
LAT
LAT
FUSE-BIT1
FUSE-BIT2
FUSE-BIT3
FUSE-BIT4
FUSE-BIT5
FUSE-BIT6
FUSE-BIT7
FUSE-BIT8
109
FUSE CELL CONTROL CIRCUIT
DPMC1
DPMC2
DPMC3
FSVS
MC4
FSWL
DPMC5
DPMC6
DPWL1
DPWL2
DPWL3
WL4
DPWL5
DPWL6
114
115'
FUSE CELL DATA PROGRAM/ ERASE CIRCUIT

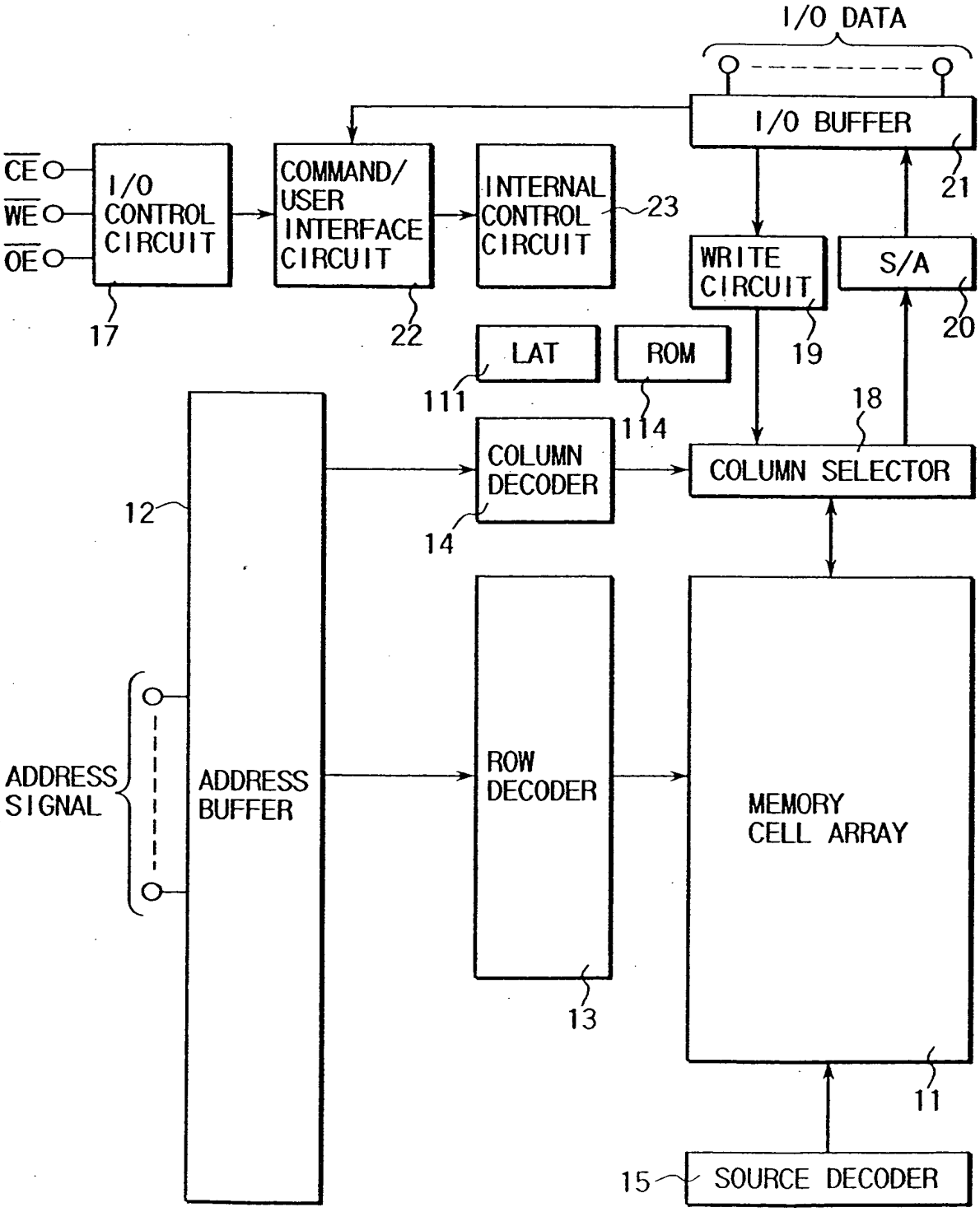

I/O DATA
I/O BUFFER
21
CE
WE
OE
I/O CONTROL CIRCUIT
17
COMMAND/ USER INTERFACE CIRCUIT
22
INTERNAL CONTROL CIRCUIT
23
WRITE CIRCUIT
19
S/A
20
LAT
111
ROM
114
18
COLUMN DECODER
14
COLUMN SELECTOR
12
ADDRESS SIGNAL
ADDRESS BUFFER
ROW DECODER
13
MEMORY CELL ARRAY
11
15
SOURCE DECODER

FIG. 32

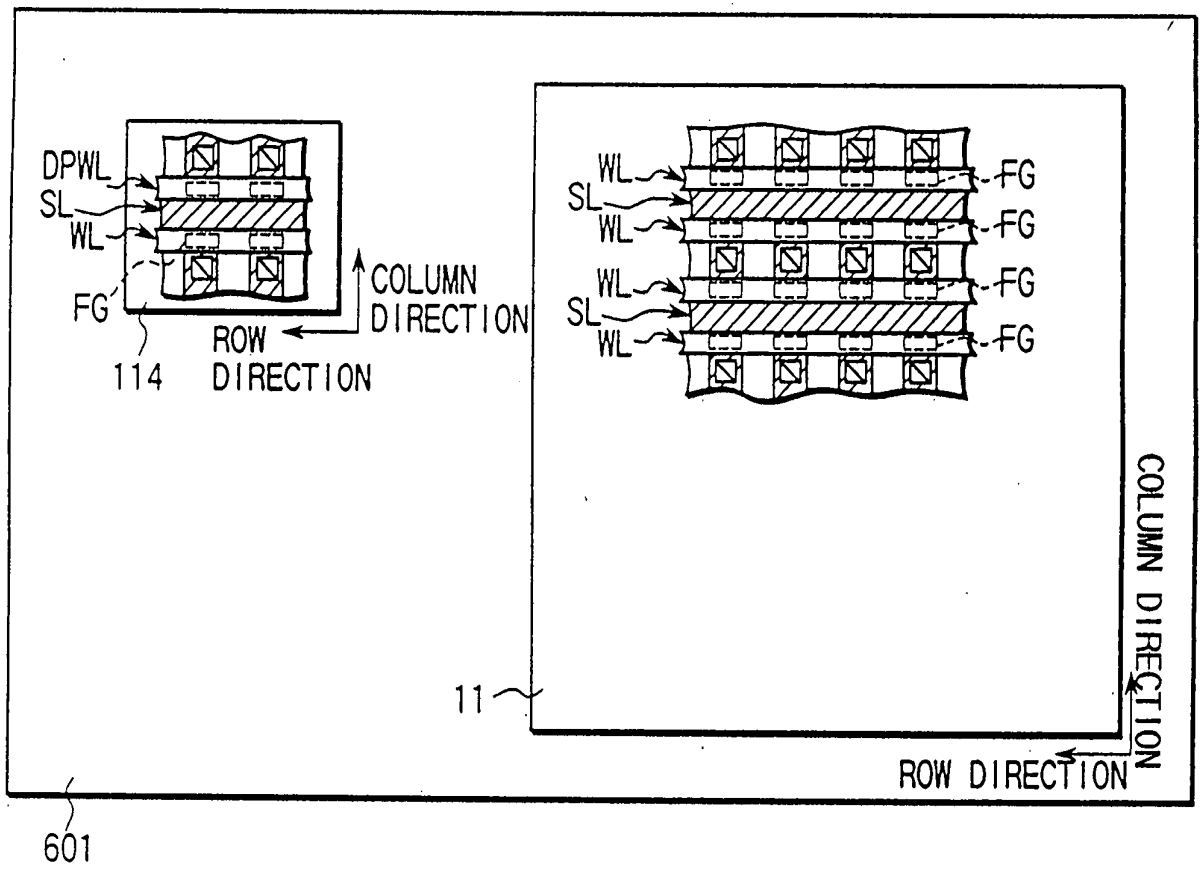

DPWL
SL
WL
FG
114
ROW DIRECTION
COLUMN DIRECTION
WL
SL
WL
WL
SL
WL
FG
FG
FG
FG
11
COLUMN DIRECTION
ROW DIRECTION
601

FIG. 33